

CLAIMS

What is claimed is:

1. A method applicable within a computer display system for providing display independence between a first display device and a second display device, wherein said first and second display devices are controlled by a common video display controller, said method comprising:

providing a first address register that is accessible by said common video display controller to display within said first display device a graphic representation of data pointed to by an address within said first address register; and

providing a second address register that is accessible by said common video display controller to display within said second display device a graphic representation of data pointed to by an address within said second address register, such that displays within said first and second display devices are independently controllable.

2. The method of claim 1, further comprising:

allocating a first frame buffer; and

selecting a dual display mode, and in response thereto, programming said first and second address registers to point to said first frame buffer.

1 3. The method of claim 2, wherein said programming said first and second address
2 registers to point to said first frame buffer during a dual display mode is followed by, in
3 response to said first and second address registers pointing to said first frame buffer,
4 displaying video data from said first frame buffer within said first and second display
5 devices.

1 4. The method of claim 1, further comprising:

2 selecting a split display mode, and in response thereto:

3 allocating a second frame buffer;

4 copying the contents of said first frame buffer to said second frame buffer; and

5 replacing the contents of said second address register to point to said second frame
6 buffer.

1 5. The method of claim 4, wherein in response to said copying the contents of said first
2 frame buffer to said second frame buffer and adjusting said second address register to point
3 to said second frame buffer, said method further comprises:

4 delivering video data corresponding to the contents of said first frame buffer to said
5 first display device; and

6 delivering video data corresponding to the contents of said second frame buffer to
7 said second display device.

1 6. The method of claim 4, wherein said second frame buffer currently stores a display
2 frame, said method further comprising:

3 selecting an alternate display frame within a video memory device; and

4 actuating a static display mode, and in response thereto:

5 maintaining said display frame within said second frame buffer; and

6 copying said alternate display frame within said first frame buffer.

1 7. The method of claim 4, wherein said computer display system includes a display
2 sequence comprising a plurality of display frames within a video memory device, said
3 method further comprising:

4 selecting an M^{th} display frame from within said display sequence;

5 actuating a split sequence display mode;

6 setting a sequence displacement value equal to N ; and

7 in response to said actuating a split sequence display mode and setting a sequence
8 displacement value equal to N :

9 copying said M^{th} display frame into said first frame buffer; and

10 copying an $(M-N)^{\text{th}}$ display frame into said second frame buffer.

1 8. An apparatus applicable within a computer display system for providing display
2 independence between a first display device and a second display device, wherein said first
3 and second display devices are controlled by a common video display controller, said
4 apparatus comprising:

5 processing means for providing a first address register that is accessible by said
6 common video display controller to display within said first display device a graphic
7 representation of data pointed to by an address within said first address register; and

8 processing means for providing a second address register that is accessible by said
9 common video display controller to display within said second display device a graphic
10 representation of data pointed to by an address within said second address register, such that
11 displays within said first and second display devices are independently controllable.

1 9. The apparatus of claim 8, further comprising:

2 processing means for allocating a first frame buffer; and

3 processing means for selecting a dual display mode, and in response thereto,
4 programming said first and second address registers to point to said first frame buffer.

1 10. The apparatus of claim 9, further comprising processing means responsive to said
2 first and second address registers pointing to said first frame buffer for displaying video data
3 from said first frame buffer within said first and second display devices.

1 11. The apparatus of claim 8, further comprising:

2 processing means for selecting a split display mode;

3 processing means for allocating a second frame buffer;

4 processing means for copying the contents of said first frame buffer to said second
5 frame buffer; and

6 processing means for replacing the contents of said second address register to point
7 to said second frame buffer.

1 12. The apparatus of claim 11, further comprising processing means responsive to
2 copying the contents of said first frame buffer to said second frame buffer and adjusting said
3 second address register to point to said second frame buffer, for:

4 delivering video data corresponding to the contents of said first frame buffer to said
5 first display device; and

6 delivering video data corresponding to the contents of said second frame buffer to
7 said second display device.

1 13. The apparatus of claim 11, wherein said second frame buffer currently stores a
2 display frame, said apparatus further comprising:

3 processing means for selecting an alternate display frame within a video memory
4 device;

5 processing means for actuating a static display mode;

6 processing means for maintaining said display frame within said second frame buffer;
7 and

8 processing means for copying said alternate display frame within said first frame
9 buffer.

1 14. The apparatus of claim 11, wherein said computer display system includes a display
2 sequence comprising a plurality of display frames within a video memory device, said
3 apparatus further comprising:

4 processing means for selecting an M^{th} display frame from within said display
5 sequence;

6 processing means for actuating a split sequence display mode;

7 processing means for setting a sequence displacement value equal to N ; and

8 processing means responsive to said actuating a split sequence display mode and
9 setting a sequence displacement value equal to N for:

10 copying said M^{th} display frame into said first frame buffer; and

11 copying an $(M-N)^{\text{th}}$ display frame into said second frame buffer.

1 15. The apparatus of claim 8, wherein said computer display system includes a central
2 processing unit, said apparatus further comprising processing means for processing data
3 within said central processing unit for generating video image data displayable on said first
4 and second display devices.

1 16. The apparatus of claim 8, wherein said second display device is a cathode ray tube
2 (CRT) display device, said apparatus further comprising processing means for converting

3 digitally encoded data addressed by said second frame buffer address register into analog data
4 for presentation on said CRT display device.

1 17. A program product applicable within a computer display system for providing display
2 independence between a first display device and a second display device, wherein said first
3 and second display devices are controlled by a common video display controller, said
4 program product comprising:

5 instruction means for providing a first address register that is accessible by said
6 common video display controller to display within said first display device a graphic
7 representation of data pointed to by an address within said first address register; and

8 instruction means for providing a second address register that is accessible by said
9 common video display controller to display within said second display device a graphic
10 representation of data pointed to by an address within said second address register, such that
11 displays within said first and second display devices are independently controllable.

1 18. The program product of claim 17, further comprising:

2 instruction means for allocating a first frame buffer; and

3 instruction means for selecting a dual display mode, and in response thereto,
4 programming said first and second address registers to point to said first frame buffer.

1 19. The program product of claim 18, further comprising instruction means responsive
2 to said first and second address registers pointing to said first frame buffer for displaying
3 video data from said first frame buffer within said first and second display devices.

1 20. The program product of claim 17, further comprising:

2 instruction means for selecting a split display mode;

3 instruction means for allocating a second frame buffer;

4 instruction means for copying the contents of said first frame buffer to said second
5 frame buffer; and

6 instruction means for replacing the contents of said second address register to point
7 to said second frame buffer.

1 21. The program product of claim 20, further comprising instruction means responsive
2 to copying the contents of said first frame buffer to said second frame buffer and adjusting
3 said second address register to point to said second frame buffer, for:

4 delivering video data corresponding to the contents of said first frame buffer to said
5 first display device; and

6 delivering video data corresponding to the contents of said second frame buffer to
7 said second display device.

1 22. The program product of claim 20, wherein said second frame buffer currently stores
2 a display frame, said program product further comprising:

3 instruction means for selecting an alternate display frame within a video memory
4 device;

5 instruction means for actuating a static display mode;

6 instruction means for maintaining said display frame within said second frame buffer;
7 and

8 instruction means for copying said alternate display frame within said first frame
9 buffer.

1 23. The program product of claim 20, wherein said computer display system includes a
2 display sequence comprising a plurality of display frames within a video memory device, said
3 program product further comprising:

4 instruction means for selecting an M^{th} display frame from within said display
5 sequence;

6 instruction means for actuating a split sequence display mode;

7 instruction means for setting a sequence displacement value equal to N ; and

8 instruction means responsive to said actuating a split sequence display mode and
9 setting a sequence displacement value equal to N for:

10 copying said M^{th} display frame into said first frame buffer; and

11 copying an $(M-N)^{\text{th}}$ display frame into said second frame buffer.